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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/667,235 | 09/17/2003 | Krishna M. Desai | POU920020104US1 | 6995 |

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| EXAMINER | |
|---|---|
| PATEL, HETUL B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/667,235 | DESAI ET AL. | |
| | Examiner | Art Unit | |
| | Hetul Patel | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 15, 2006 has been entered and carefully considered. Claims 1, 8 and 12 have been amended and claims 1-14 are again presented for examination.

2. Applicant's arguments filed on May 15, 2006 have been fully considered but they are not deemed to be moot in view of new ground rule rejection.

### *Claim Objections*

3. Claims 1 and 8 are objected to because of the following informalities:

The difference between the first and second operation modes is not clearly claimed in the claim 8 of this application. Lines 4-13 of claim 8 claims that in both the first and second operational modes, both the cache directory and cache array are updated regardless of a cache hit or a cache miss.

Claim 1 recites the limitation "said placing said cache in the second operational mode" in lines 9-10. The phrases "said placing", which refers to "placing said cache in a

memory mode" and "said placing said cache in the second operational mode" are inconsistent.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi et al. (USPN: 5,708,803) hereinafter, Ishimi in view of Baron et al. (USPN: 5,586,293) hereinafter, Baron.

As per claim 8, Ishimi teaches a system of writing to cache comprising: a cache directory (the tag unit 2 in Fig. 3); a cache array (the data unit 3 in Fig. 3); control logic (i.e. the valid bit unit 90 in Fig. 3) for writing a valid field (i.e. a valid bit) and an address to said cache directory and data to said cache array. As described above under the Claim Objection heading, in both the first and second operational modes, both the cache directory and cache array are updated regardless of a cache hit or a cache miss. Ishimi discloses these limitations at Col. 5, lines 14-17: when a cache miss occurs, external data bus is accessed and the data is fetched, i.e. from the further storage/memory; and when the cache hit occurs, the data is accessed from the cache. Similarly, in the normal cache operating mode, when the cache miss occurs, the data is written both in cache memory (i.e. by updating the cache directory with the contents of

the target address) and the further storage/memory; and when the cache hit occurs, the data is updated only in the cache memory (e.g. see Col. 12, lines 40-43; Col. 13, lines 24-32 and Col. 5, lines 14-17). Furthermore, Ishimi teaches about placing the cache in the second operational mode by setting a memory mode bit (i.e. 9 in Fig. 4). However, Ishimi does not teach the further limitation that the memory mode bit is logically combined with a write command pulse to generate the memory mode write pulse and performing the logical operation of the memory mode write pulse and a cache hit write pulse, wherein in the absence of a cache hit write pulse, the data is written to the cache in the presence of the memory mode write pulse. Baron, on the other hand, teaches about placing/switching the cache (i.e. the internal program memory 10 in Fig. 1) in the second operational mode (i.e. the memory mode) by logically combining (i.e. by switch 22 in Fig. 1) the memory mode bit (i.e. the cache enable signal 16 in Fig. 1) with a write command pulse (i.e. the PAB in Fig. 1) and performing the logical operation of the memory mode write pulse and a cache hit write pulse. In the absence of a cache hit write pulse, the data is written to the cache (i.e. the internal program memory 10 in Fig. 1) in the presence of the memory mode write pulse (e.g. see Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to place the cache in the second operational mode and the writing the data in the cache in the Ishimi's system as taught by Baron. In doing so, the data is written to the cache based on not only the memory mode bit (i.e. the cache enable signal 16 in Fig. 1) but also based on the memory mode write pulse so in the in the absence of a cache hit write pulse, the data can be written to the cache based on it.

As per claim 9, the combination of Ishimi and Baron teaches the claimed invention as described above and furthermore, Ishimi teaches that said second operational mode is designated by a memory mode bit (DM bit of a BMC register 900) (e.g. se Col. 5, lines 5-11 and Fig. 3).

As per claim 10, the combination of Ishimi and Baron teaches the claimed invention as described above and furthermore, Ishimi teaches that the system further comprising: a device control register (the BMC register 900 in Fig. 3) storing said memory mode bit (e.g. se Col. 5, lines 5-11 and Fig. 3).

As per claim 1, Ishimi teaches a method of writing to cache comprising: initiating a write operation to a cache; in a first operational mode: detecting the presence or absence of a write miss; if a write miss is absent, writing data to said cache; if a write miss is present, retrieving said data from a further memory and writing said data to said cache (e.g. see Col. 12, lines 40-43 and Col. 13, lines 24-32); in a second operational mode: placing said cache in a memory mode; writing said data to said cache and updating the cache directory with the contents of the target address regardless of whether a write miss is present or absent (e.g. see Col. 5, lines 14-17). However, Ishimi does not teach the further limitation that the memory mode bit is logically combined with a write command pulse to generate the memory mode write pulse and performing the logical operation of the memory mode write pulse and a cache hit write pulse, wherein in the absence of a cache hit write pulse, the data is written to the cache in the presence of the memory mode write pulse. Baron, on the other hand, teaches about placing/switching the cache (i.e. the internal program memory 10 in Fig. 1) in the

second operational mode (i.e. the memory mode) by logically combining (i.e. by switch 22 in Fig. 1) the memory mode bit (i.e. the cache enable signal 16 in Fig. 1) with a write command pulse (i.e. the PAB in Fig. 1) and performing the logical operation of the memory mode write pulse and a cache hit write pulse. In the absence of a cache hit write pulse, the data is written to the cache (i.e. the internal program memory 10 in Fig. 1) in the presence of the memory mode write pulse (e.g. see Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to place the cache in the second operational mode and the writing the data in the cache in the Ishimi's system as taught by Baron. In doing so, the data is written to the cache based on not only the memory mode bit (i.e. the cache enable signal 16 in Fig. 1) but also based on the memory mode write pulse so in the in the absence of a cache hit write pulse, the data can be written to the cache based on it.

As per claims 2-3, see arguments with respect to the rejection of claims 9 and 10, respectively. Claims 2 and 3 are also rejected based on the same rationale as the rejection of claims 9 and 10, respectively.

5. Claims 4-5 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi in view of Baron, further in view of Dosaka et al. (USPN: 6,347,063) hereinafter, Dosaka.

As per claim 11, the combination of Ishimi and Baron teaches the claimed invention as described above. However, neither Ishimi not Baron teach that the second operational mode is designated by address bits contained within said address. Dosaka,

on the other hand, teaches that the second operational mode (i.e. write protect control mode) is designated by address bits (i.e. 3 most significant row address bits) contained within the address (e.g. see Col. 61, lines 25-50). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to use the address bits of the address to designate the second operational mode as taught by Dosaka in the system taught by the combination of Ishimi and Baron. In doing so, just by examining the appropriate address bits of the address, the operational mode of the cache can be determined.

As per claim 12, the combination of Ishimi, Baron and Dosaka teaches the claimed invention as described above and furthermore, Dosaka teaches that said address bits contained within said address include the high order address bits (i.e. Ad2 and Ad3) (e.g. see Col. 61, lines 25-50). Keeping high order address bits equal to '1111' for designating the second operational mode is a system dependent feature. Since neither applicant nor specification specifically disclose that using some other value other than '1111' in the high order address bits would change the system functionality or performance, therefore, any number of high order bits can be selected for setting to any specific value for designating the second operation mode.

As per claims 4-5, see arguments with respect to the rejection of claims 11 and 12, respectively. Claims 4 and 5 are also rejected based on the same rationale as the rejection of claims 11 and 12, respectively.

6. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi in view of Baron, further in view of Anthony et al. (USPN: 4,885,680) hereinafter, Anthony.

As per claim 14, the combination of Ishimi and Baron teaches the claimed invention as described above but failed to teach that the control logic invalidates cache directory entries associated with writing said data in response to a select all bins bit. However, Anthony teaches that when the cacheability of the temporarily cacheable data changes from cacheable to non-cacheable, a single instruction is issued to cause the cache to invalidate all marked data. When an "invalidate marked data" (similar to the claimed "a select all bins bit") instruction is received, the cache controls sweep through the entire cache directory and invalidate any cache line that has the "marked data bit" set in a single pass (e.g. see the abstract and claim 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Anthony in the system taught by the combination of Ishimi and Baron. In doing so, it improves system performance as result of reduced memory latency and improved coherence of data.

As per claim 7, see arguments with respect to the rejection of claim 14. Claim 7 is also rejected based on the same rationale as the rejection of claim 14.

7. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ishimi and Baron.

As per claim 13, the combination of Ishimi and Baron teaches the claimed invention as described above but failed to teach that said control logic retrieves a bin identifier from said address, said bin identifier designating said compartment of said cache where said data is to be written, i.e. the control logic retrieves which cache line needs to be written/updated in the cache. However, many different cache replacement algorithms, such as LRU, MRU, FIFO, LIFO etc. the cache controller retrieves the cache location that needs to replaced, are well-known and notorious old in the art. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

As per claim 6, see arguments with respect to the rejection of claim 13. Claim 6 is also rejected based on the same rationale as the rejection of claim 13.

## *Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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